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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Martin VORBACH et al.

Serial No. : 09/145,139

Filing Date : August 28, 1998

For : INTERNAL BUS SYSTEM FOR DFPS AND UNITS
WITH TWO- OR MULTI-DIMENSIONAL
PROGRAMMABLE CELL ARCHITECTURES, FOR
MANAGING LARGE VOLUMES OF DATA WITH A HIGH
INTERCONNECTION COMPLEXITY

Group Art Unit : 2781

Examiner : T. Vo

Assistant Commissioner
for Patents
Washington, D.C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

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AMENDMENT

SIR:

This paper addresses the Office Action dated August 11, 2000. Initially, kindly amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

22. (Twice Amended) The method according to claim 18 [19], wherein the module having the multi-dimensional cell architecture includes at least one of a field programmable gate array and a dynamically configurable gate array.

23. (Twice Amended) The method according to claim 18 [19], wherein the module having the multi-dimensional cell architecture includes a module having a two-dimensional programmable cell architecture.